storage device, and a cache directory identifying data in said direct access storage device for which copies are stored in said cache memory, and identifying memory locations in said cache memory where each said copy is stored,

responding to a request for access to a storage device location for which a copy is stored in the cache memory, by accessing the copy stored in the cache memory,

responding to a request for access to a desired storage device location for which a copy is not stored in the cache memory, by accessing said desired storage device location from said storage device, and

responding to a change in said total available cache memory capacity by altering said cache directory.

22. The method of claim 21 wherein in response to an increase in the total cache memory capacity, the method further comprises modifying said cache directory to identify memory locations in said cache memory where copies of data from said direct access storage device may be stored, and then storing, in said cache memory, copies of data retrieved from said direct access storage device.

23. The method of claim 21 wherein in response to a reduction in the total cache memory capacity, the method further comprises modifying said cache directory to no longer identify memory locations that are not available in said cache memory.

Please add new claims 45-57 as follows.

45. A cache control circuit for a direct access storage device having a plurality of addressable locations, for controlling a cache memory having a total available memory capacity, storing copies of data retrieved from said direct access storage device, and a cache directory identifying data in said direct access storage device for which copies are stored in said cache memory, and identifying memory locations in said cache memory where each said copy is stored, the cache control circuit performing the steps of:

responding to a request for access to a storage device location for which a copy is stored in the cache memory, by accessing the copy stored in the cache memory,

responding to a request for access to a desired storage device location for which a copy is not stored in the cache memory, by accessing said desired storage device location from said storage device, and

responding to a change in said total available cache memory capacity by altering said cache directory.

46. The cache control circuit of claim 45 wherein in response to an increase in the total cache memory capacity, the cache control circuit modifies said cache directory to identify memory locations in said cache memory where copies of data from said direct access storage device may be stored, and then storing, in said cache memory, copies of data retrieved from said direct access storage device.

47. The cache control circuit of claim 45 wherein in response to a reduction in the total cache memory capacity, the cache control circuit modifies said cache directory to no longer identify memory locations that are not available in said cache memory.

48. The cache control circuit of claim 45 wherein said control circuit monitors accesses to data for which copies are stored in the cache memory.

49. The cache control circuit of claim 48 wherein said control circuit monitors accesses to data by maintaining a LRU queue in which data are ordered from most to least recently used.

50. The cache control circuit of claim 49 wherein said control circuit monitors accesses to data by maintaining statistics on types of accesses made to data.

51. The cache control circuit of claim 50 wherein wherein said control circuit maintains statistics on types of accesses made to data by maintaining a counter associated with blocks of data, said counters being credited or penalized in response to types of accesses made to the associated block of data.

52. The cache control circuit of claim 51 wherein wherein said control circuit maintains statistics by crediting a counter by a predetermined credit in response to a read to a block of data associated with said counter, and penalizing said counter by a predetermined penalty in response to a write to a block of data associated with said counter.

53. The cache control circuit of claim 51 wherein said control circuit

identifies a least advantageous block of data for which a copy is stored in the cache memory, based on previously monitored accesses to blocks of data, and

as part of responding to a request for access to a desired storage device location for which a copy is not stored in the cache memory, retrieves from said direct access storage device a block of data including said desired storage device location, and stores the block of data retrieved from said storage device, in place of the copy in said cache memory of said least advantageous block of data.

54. The cache control circuit of claim 48 wherein said control circuit monitors accesses to data for which copies are not stored in the cache memory.

55. A program product, comprising:

(a) a program configured to perform a method of caching data for a direct access storage device having a plurality of addressable locations, comprising the steps of:

storing, in a cache memory having a total available memory capacity, copies of data retrieved

from said direct access storage device, and a cache directory identifying data in said direct access storage device for which copies are stored in said cache memory, and identifying memory locations in said cache memory where each said copy is stored,

responding to a request for access to a storage device location for which a copy is stored in the cache memory, by accessing the copy stored in the cache memory,

responding to a request for access to a desired storage device location for which a copy is not stored in the cache memory, by accessing said desired storage device location from said storage device, and

responding to a change in said total available cache memory capacity by altering said cache directory, and

(b) a signal bearing media bearing the program.

56. The program product of claim 55, wherein the signal bearing media is a transmission type media.

57. The program product of claim 55 wherein the signal bearing media is a recordable media.